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Patent/Publication No. 318983

Publication Date 1997/11/01

Application Date 1996/12/23

Application No. 085115906

Certification_Number 090280

IPC *H04J-013/00*

Applicant INTERDIGITAL TECHNOLOGY
CORP US

Priority Number

1995-06-30	US	60/000775
1996-06-27	US	08/669775

Individual N

Patent Right Change

Application Number	085115906
Date of Update	20090520
Licensing	No
Mortgage	No
Transfer	No
Succession	No
Trust	No
Opposition	No
Invalidation	No
Cessation	
Revocation	
Issue date of patent right	19971101
Patent Grant date	20161222
Maintenance fee due	20091031
Years of maintenance paid	012

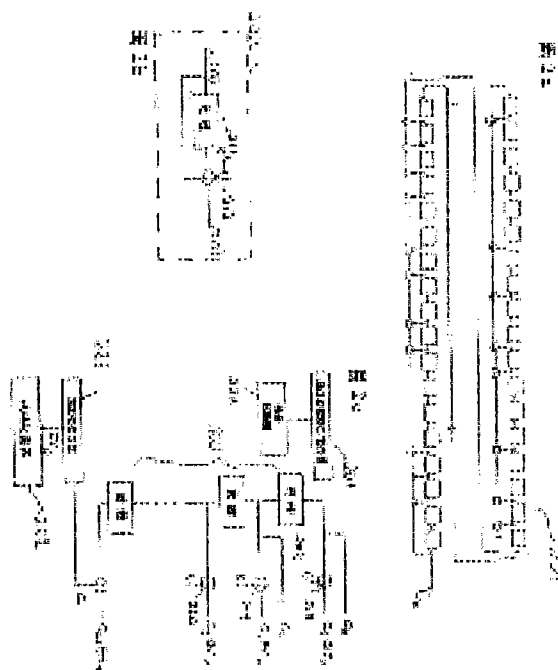


Figure 1

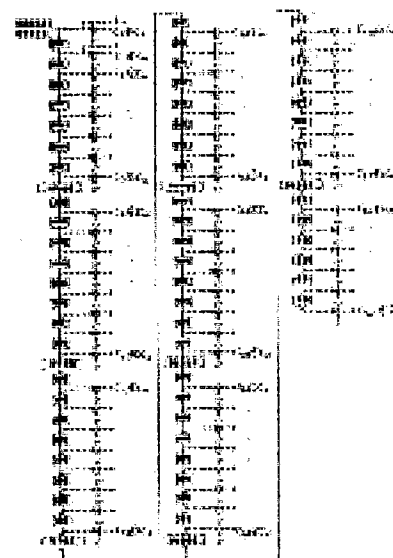


Figure 2

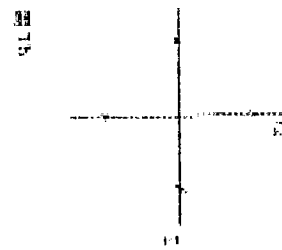
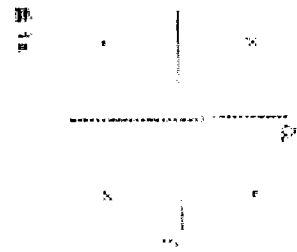
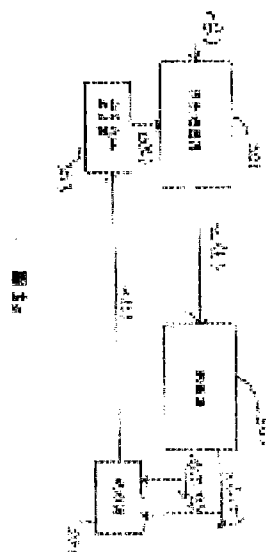
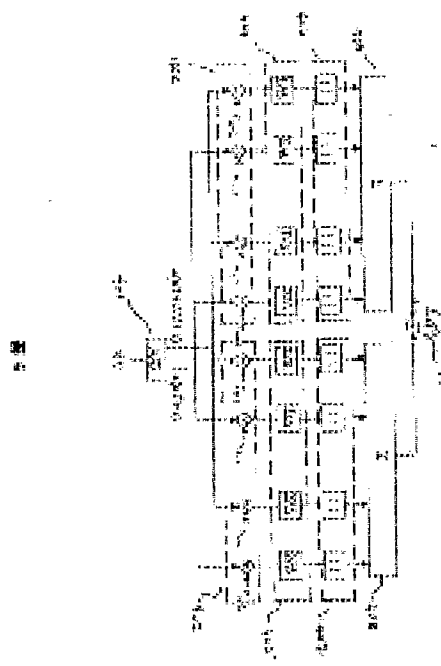


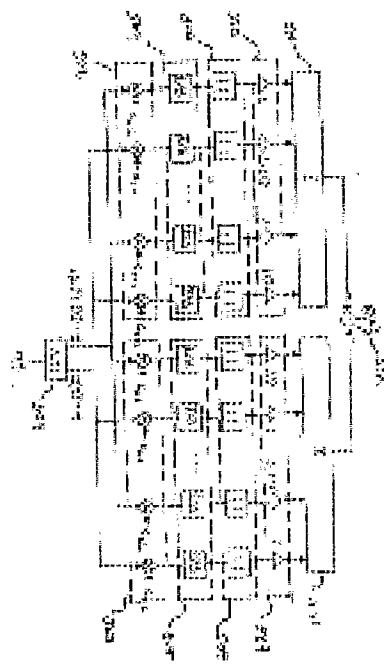
Figure 3





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圖 13



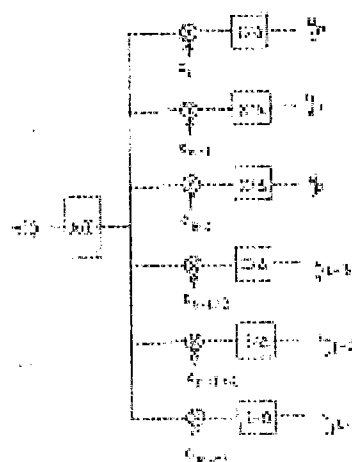
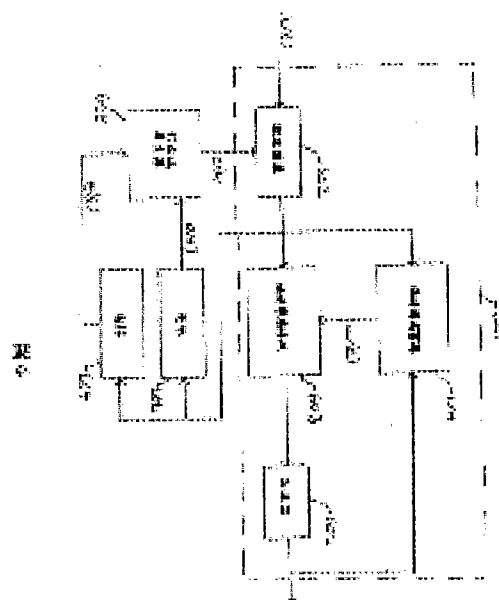
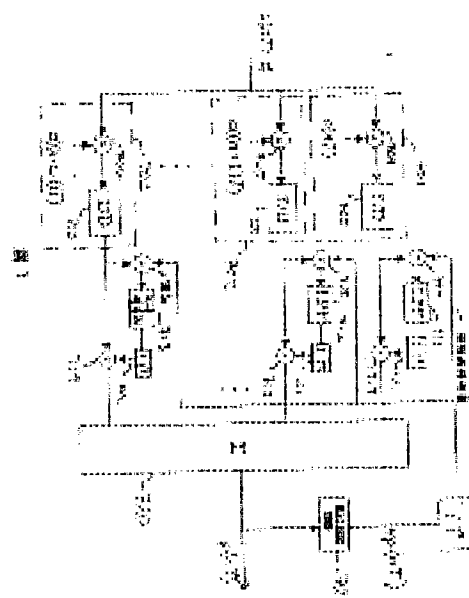


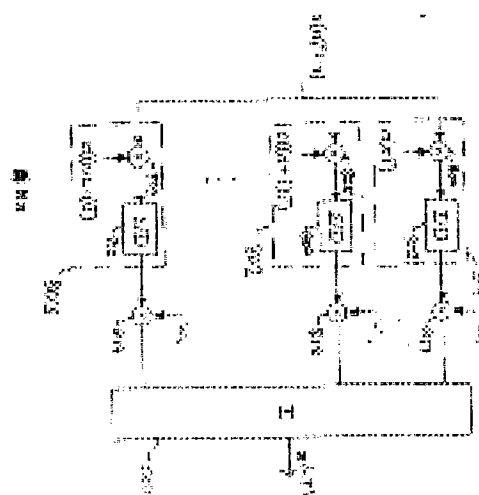
Fig. 5b

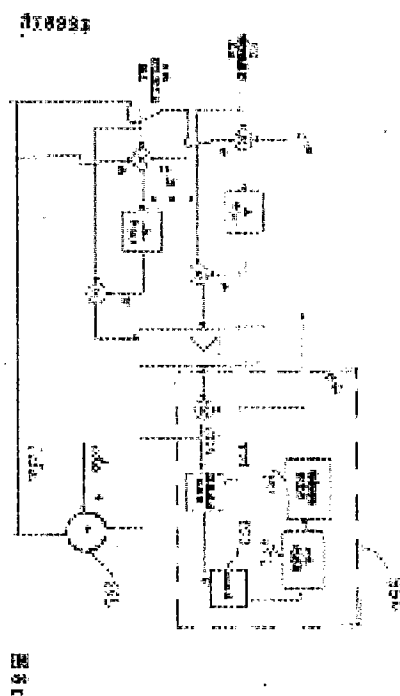
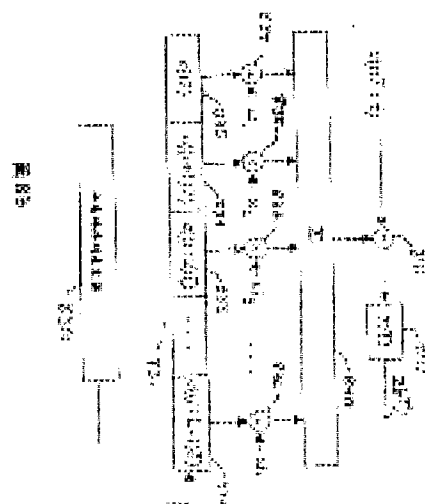
Fig. 5c

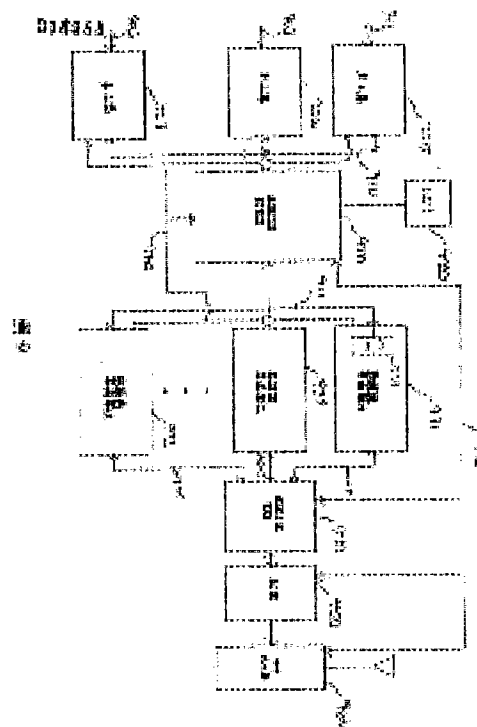
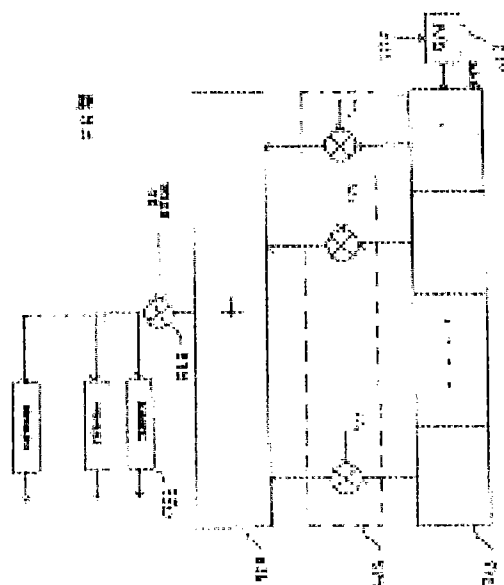


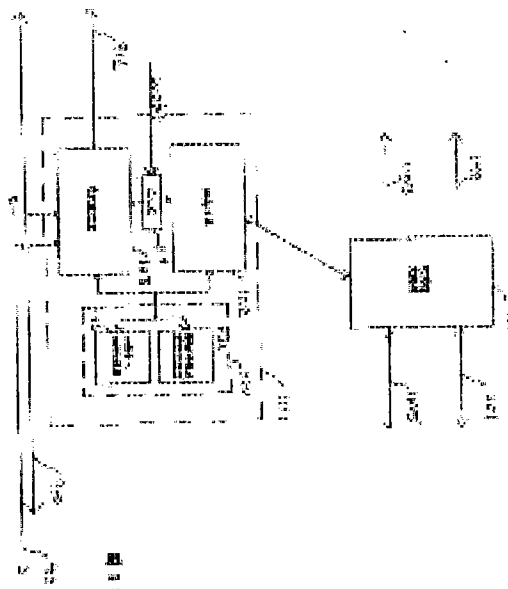
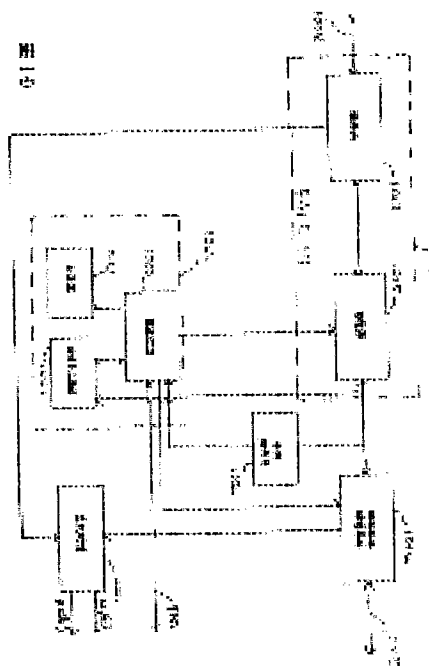


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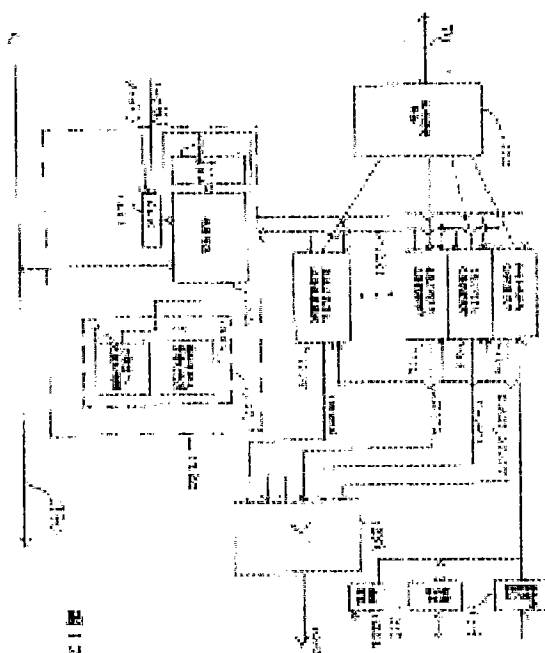


Figure 1

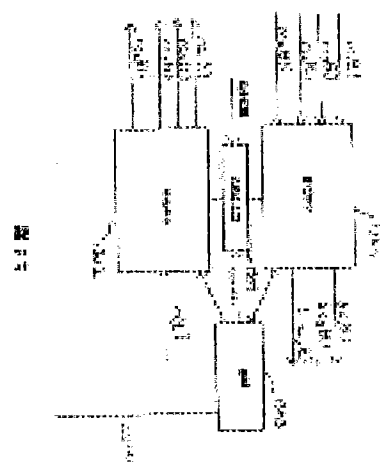


Figure 2

H. 1-4

The block diagram illustrates the system architecture. It features a central vertical bus labeled "System Bus". On the left side, there are three main functional blocks: "User Interface", "Database", and "Control Unit". The "User Interface" block is connected to the "System Bus" and also has a direct connection to the "Database". The "Database" block is connected to the "System Bus" and the "Control Unit". The "Control Unit" is connected to the "System Bus" and the "Database". On the right side, there are five processing units arranged vertically, each connected to the "System Bus": "Unit 1", "Unit 2", "Unit 3", "Unit 4", and "Unit 5". Each unit has its own local storage or cache, labeled "Cache 1" through "Cache 5" respectively, which are also connected to the "System Bus".

7. 13.

Figure 16

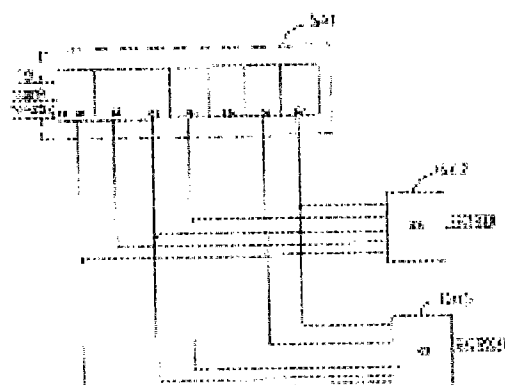


Figure 16

Figure 17

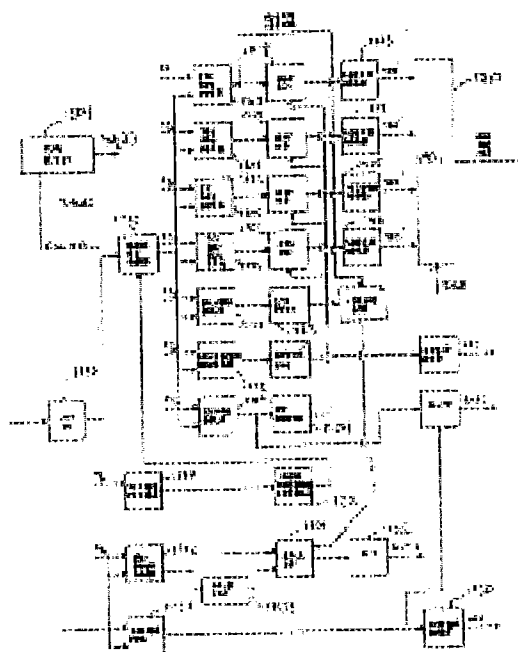


Figure 17

FIG. 10

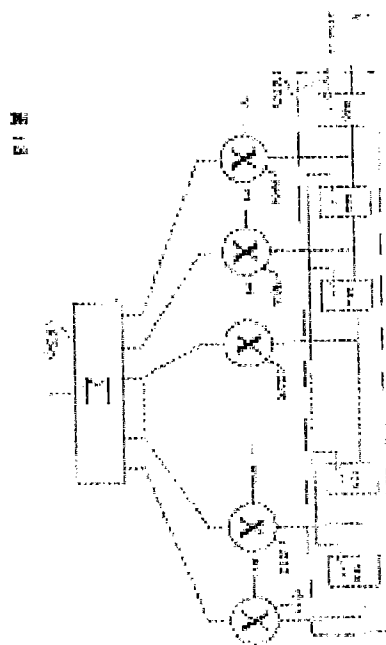
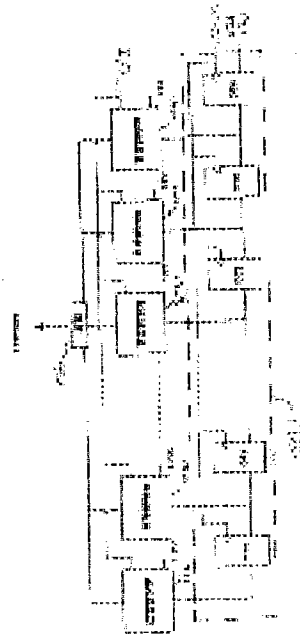


FIG. 11



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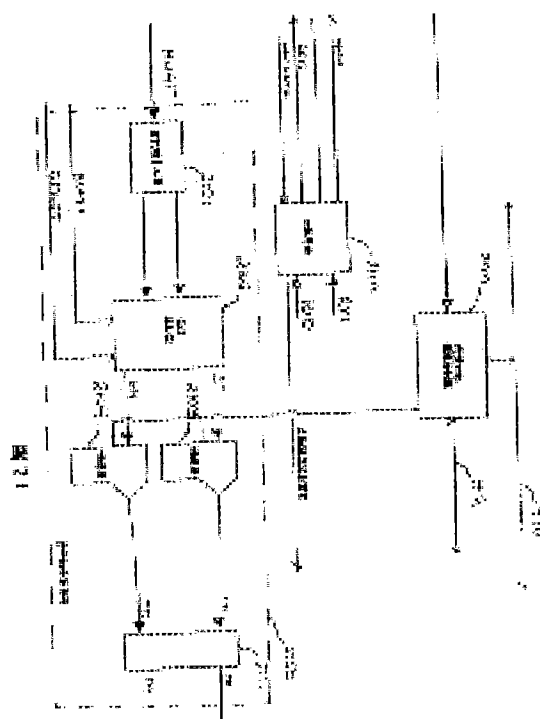
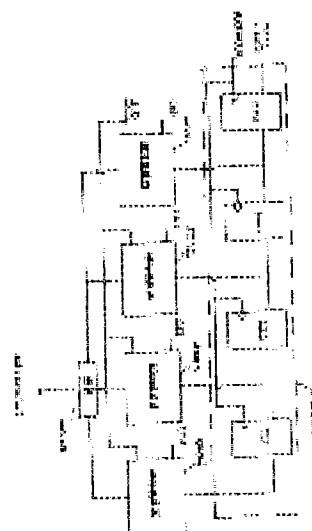


FIG. 10

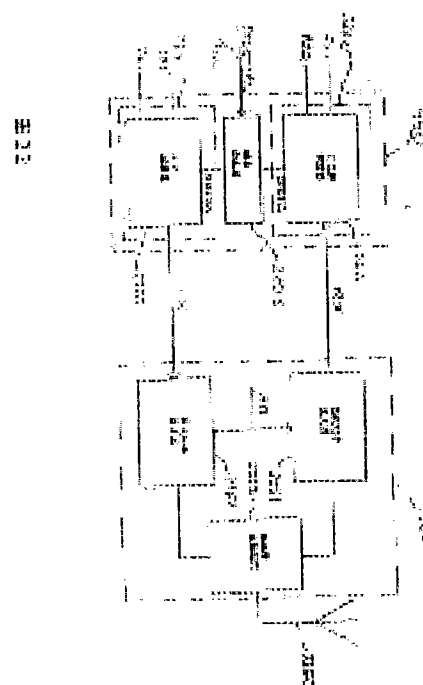


FIG. 11

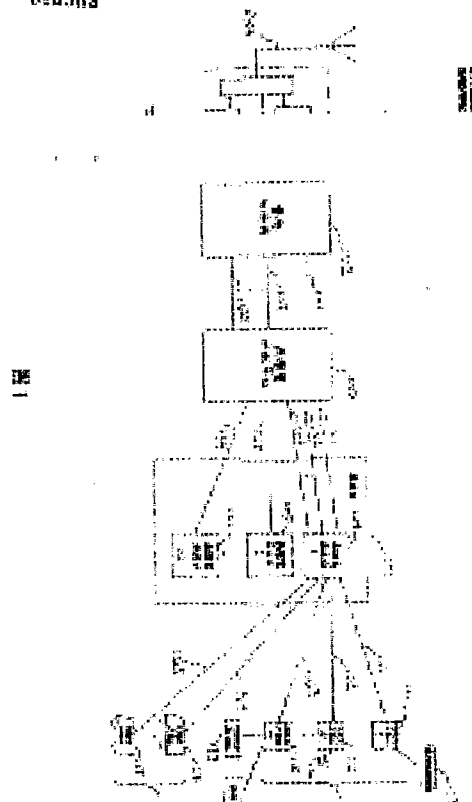


圖 24

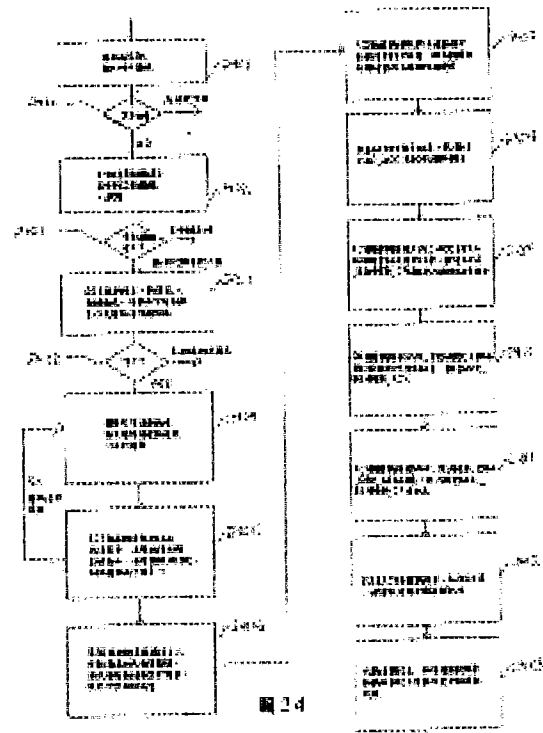
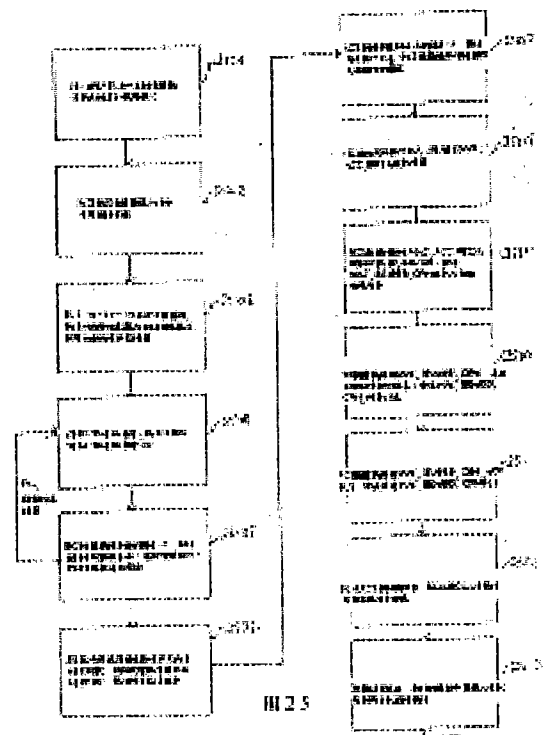


圖 25



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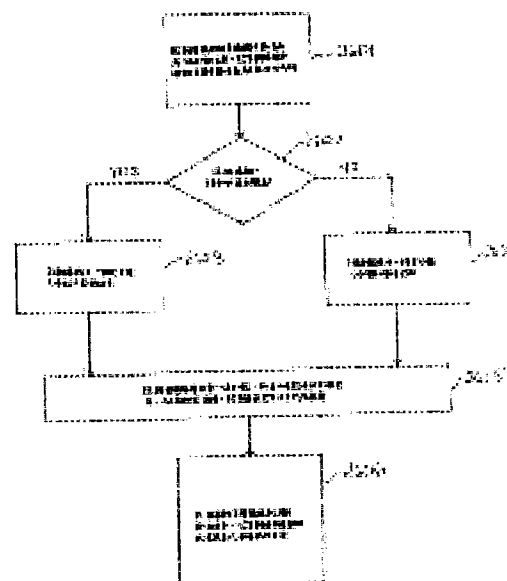


圖 26

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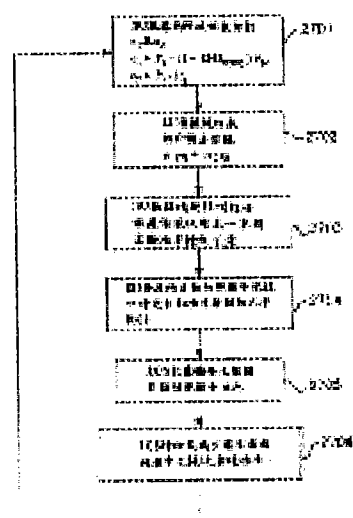


圖 27

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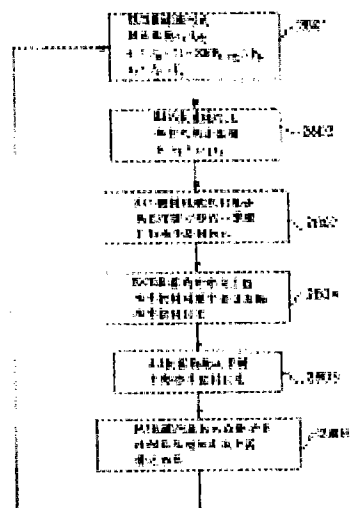


圖 28

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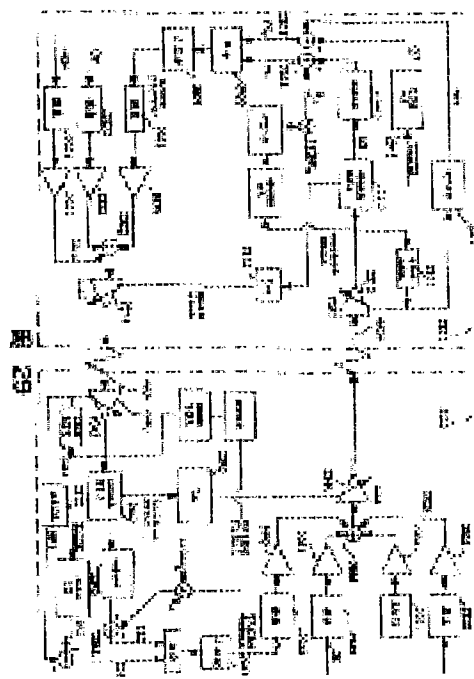
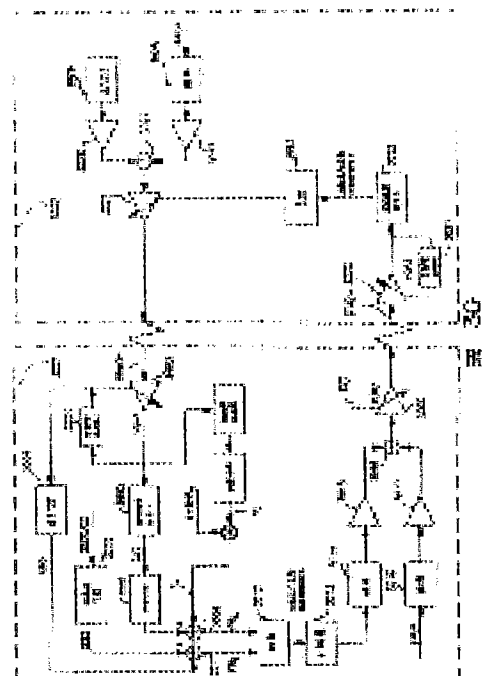


圖 15A



公告本

申請日期	85. 12. 23.
案 號	85115906
類 別	404T ¹³ Int. C16

(以上各欄由本局填註)

A4
C4

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發明專利說明書

一、發明 名稱	中 文	分碼多向近接通訊系統
	英 文	"CODE DIVISION MULTIPLE ACCESS (CDMA) COMMUNICATION SYSTEM"
二、發明 人	姓 名	1. 蓋瑞·洛普 2. 約翰·柯瓦斯基 3. 費斯·歐路特克 4. 艾維·希維伯格 5. 羅伯·瑞吉 6. 麥克·露蒂 7. 亞歷山大·瑪拉 8. 亞歷山大·賈奎斯
	國 籍	1. 2. 4. 5. 6. 7. 8. 均美國 3. 土耳其
三、申請人	住、居所	1. 美國紐約州森特波市華盛頓路130號 2. 美國紐約州希普斯德市希伯街65號 3. 美國紐約州華盛頓港市米德奈克路1474號 4. 美國紐約州康麥克市木棉道路40號 5. 美國紐約州亨丁頓市丹樂普路51-A號 6. 美國紐約州希克利夫市唐寧街15號 7. 美國紐約州紐約市費吉區11號 8. 美國紐約州米諾拉市伯奇伍區6號40室
	代 表 人 姓 名	D·瑞吉萊·包吉諾